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A fully Integrated Regulated Charge Pump in 1.2/2.5-V 90-nm CMOS Technology

Anass Slamti[1], Youness Mehdaoui[*1,2] and Zakia Lakhlai[1]

[1]*Computer and Interdisciplinary Physics Laboratory, USMBA, Fez, Morocco, USMBA, Fez, Morocco*
[2]*Research team in Electronics, Instrumentation and Measurements, USMS, Beni-mellal, Morocco*

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***Correspondence Info:**
Youness Mehdaoui
Computer and Interdisciplinary Physics Laboratory,
USMBA, Fez, Morocco, USMBA, Fez, Morocco

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Abstract

A fully integrated regulated charge pump is designed in 1.2/2.5-V 90-nm CMOS technology. The charge pump exploits two control schemes to provide stable output voltage with small ripple output voltage and high current load drivability. The first is automatic pumping current control scheme which optimizes the pumping current flowing through flying capacitor to reduce ripple voltage. The second is variable pumping frequency control scheme which changes pumping frequency by controlling a VCO. This charge pump delivers regulated 3.8-V output voltage from a supply voltage of 2.5-V with a flying capacitor of 590-nF, while providing 50-mA of load current. The measured output ripple voltage is less than 20-mV with a 2.2-µF load capacitor. The power efficiency is greater than 80% at the range of load current from 10 to 50-mA.

Keywords: Regulated charge pump, automatic pumping current, variable pumping frequency, high current load drivability, power efficiency.

1. Introduction

In many mixed signal integrated circuits such as EEPROMs and switched capacitor transformers, charge pumps are frequently used to provide a voltage higher than a power supply because high voltage level in a charge pump is generated by transferring charges to a capacitive load without any amplifiers or regular transformers [1]. The conventional applications have required a high voltage level with only limited current load drivability. Many approaches to the charge pump have focused on the design of Dickson charge pump such as [2]-[4]. However recent applications like USB-OTG (On-The-Go), require not only the high voltage level but also high current drivability [5].

According to [6]-[7], the output voltage has a dependence on the load current. To reduce the dependence, the regulated charge pump was proposed [8]. It generates high constant output voltage regardless of load current by employing clock blocking scheme. Figure 1 shows a conceptual schematic of conventional regulated charge pump. By using this charge pump, constant output voltage with large load current can be achieved. However large ripple voltage is incurred due to the clock blocking for large load current.

Figure 1: Schematic of a conventional regulated charge pump

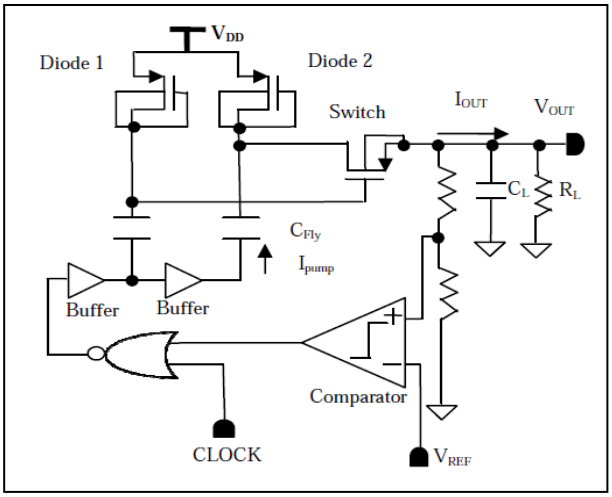
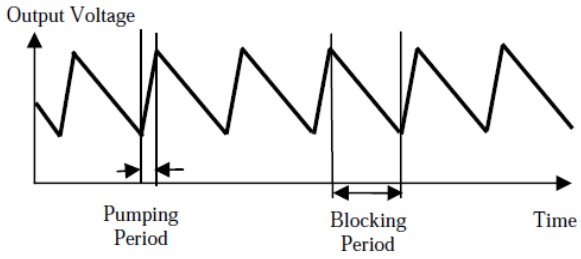


Figure 2: Operation of a conventional regulated charge pump



This work describes a design of regulated charge pump incorporating automatic pumping control schemes to reduce ripple voltage while delivering large load current. This charge pump generates regulated 3.8-V output voltage and 13.22-mV ripple voltage with 50-mA load current.

2. Conventional regulated charge pump

In the conventional charge pump, clock blocking scheme is adopted isolating the load resistor R_L which determines load current. Although its average output voltage has constant value regardless of load resistor, the large output ripple voltage is generated in pumping period and blocking period.

The operation of conventional regulated charge pump is shown in Figure 2. The load capacitor C_L is charged during only pumping period and discharged through load resistor. The output ripple voltage during pumping period [7] is determined by:

$$\Delta V_{OUT} = \frac{I_{pump}}{f_s C_L} \quad (1)$$

Where I_{pump} is the pumping current into flying capacitor which is equal to I_{OUT} in steady state, C_L is the output load capacitance and f_s is the switching frequency between pumping and blocking period.

This means that the ripple voltage is proportional to the pumping current and inversely proportional to the switching frequency. From equation (1), it is clear that either small pumping current or large output capacitor or high switching frequency is needed to achieve small ripple.

However, in practice, changing the load capacitor value is difficult when the load capacitor value is given in specification. On the other hand, simple reduction of pumping current may lose load current supplying capability. Therefore, to reduce output ripple, control of pumping current and clock frequency according to the load current is needed.

3. Proposed regulated charge pump

The proposed regulated charge pump has six main blocks to accomplish the required performance. The block diagram of the proposed charge pump is shown in Figure 3. The first block of charge pump is Main Charge Pump (MCP). It boosts voltage by using general bootstrapping scheme. The second one is Output Stage Detect Unit (OSDU). It detects output voltage level. The third one is Driving Buffer Size Control Unit (DBSCU). It controls the size of Automatic Driving Buffer (ADB). The latter is the fourth block which is reduces output ripple voltage. The fifth block is a Variable Pumping Frequency Control block. It reduces output ripple voltage and stabilizes output voltage. The sixth block is Warming-Up Stage. It prevents breakdown of transistors in MCP. The operation of proposed charge pump is explained in Figure 4.

Figure 5 shows the reduction of output ripple voltage in proposed regulated charge pump compared to conventional regulated charge pump. In case of a conventional regulated charge pump, the output voltage is independent of the load resistor, but it has large ripple voltage because it always pumps the flying capacitor with full power. However the proposed regulated charge pump makes the output voltage independent of load resistor and creates a small ripple voltage. The schematic of proposed regulated charge pump is shown in Figure 6.

3.1 Automatic pumping current control scheme

The automatic pumping current control scheme is realized by four functional blocks; MCP, OSDU, DBSCU and ADB.

Figure 3: Block diagram of propsed reguled charge pump

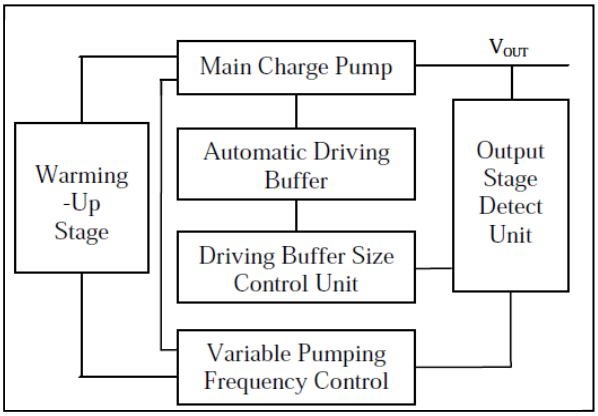


Figure 4: Operation of propsed reguled charge pump

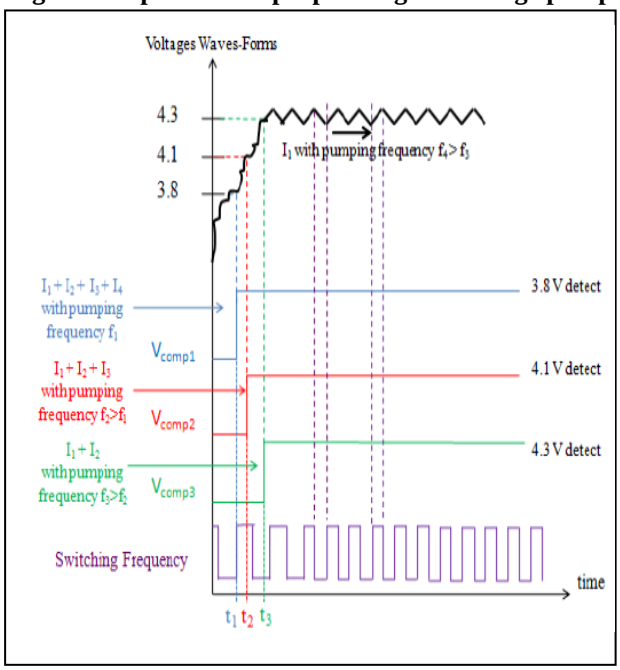
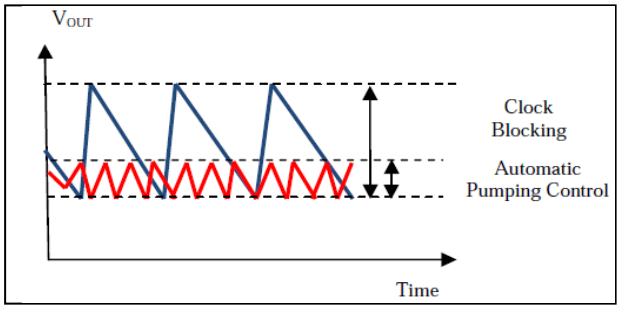


Figure 5: Reduction of ripple voltage in proposed regulated charge pump



The OSDU block detects output voltage level and informs the detected voltage level to DBSU block. Three comparators are used to detect output voltage level. Each comparator detects 3.8-V, 4.1-V and 4.3-V separately. Fig. 7 shows the schematic of this comparator. Main function of DBSU block is to control the size of ADB block. By controlling the size of automatic driving buffer, output ripple voltage can be reduced because pumping current to flying capacitor is controlled. With the outputs of 3.8-V, 4.1-V and 4.3-V detecting comparators in OSDU block, DBSCU block controls driving buffer sizes. When V_{OUT} is lower than 3.8-V, DBSCU block increases pumping current by controlling ADB block. Meanwhile, in case that V_{OUT} is higher than 4.3-V, DBSCU block reduces the magnitude of pumping current. The output ripple voltage of proposed regulated charge pump is given by

$$\Delta V_{OUT} = \frac{\sum_{n=1}^{4} I_n}{f_s C_L} \quad (2)$$

Figure 6: Schematic of proposed regulated charge pump

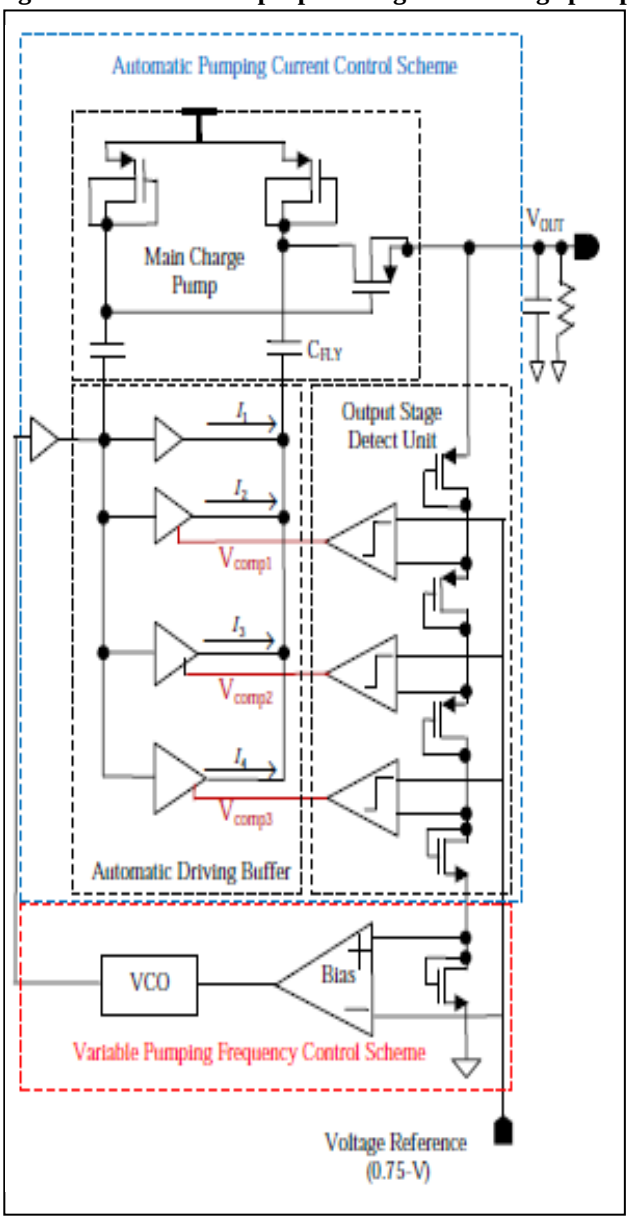
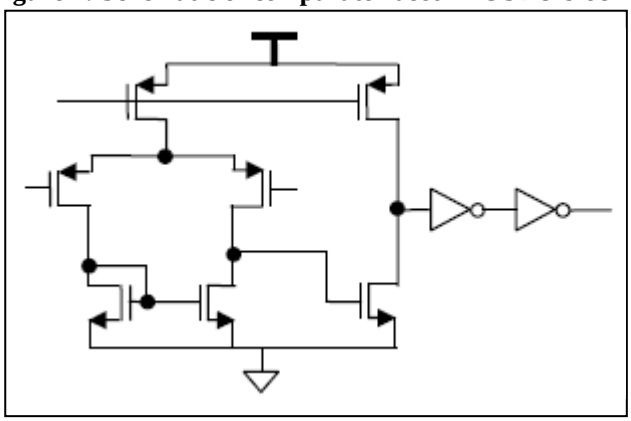


Figure 7: Schematic of comparator used in OSDU block



3.2 Variable pumping frequency control scheme

To enhance the performance of regulated charge pump, such as stable output voltage and small ripple voltage, comparing with the Dickson booster, variable

pumping frequency control scheme is used. This scheme has been developed in previous works [9]. In equation (1), the switching clock frequency of the charge pump is related to the output ripple voltage. The switching frequency is same as clock frequency because this charge pump repeats the current pumping every clock cycle, while the conventional charge pump with the clock blocking scheme suspends the operation for the blocking period. Figure 8 shows the relationship between output ripple and clock frequency. As equation (1) implies, the ripple is inversely proportional to the pumping frequency. The block diagram of variable pumping frequency control scheme is shown in Figure 6. A current Starved Voltage Controlled Oscillator (CSVCO) [10] shown in Figure 9a generates a clock signal which determines the pumping frequency. After the output voltage is detected, a bias block compares the voltage divided by MOSFET resistors with a accuracy reference voltage and linearly converts to the control voltage of the CSVCO. Operating clock frequency of proposed charge pump changes from 700-KHz to 900-KHz as the output voltage rises. The frequency of the CSVCO output signal is a linear function of its input signal, it is expressed as:

$$f_s = \frac{I_{D5R}}{NC_{tot}V_{DD}} \qquad (3)$$

Where I_{D5R} is a drain current of MOSFET MR5 expressed as

$$I_{D5R} = 2nU_T^2K_n\left(\frac{W}{L}\right)\left(1+\frac{V_{inVCO}-V_S-V_{thn}}{nU_T}\right) \qquad (4)$$

C_{tot} is the total capacitance between the output of the first inverter and the input of the inverter that follows immediately. **N** is the number of stages (number of CS_INV).

n is the subthreshold factor.

U_T is the thermal voltage.

V_{thn} is the threshold voltage of MOSFET MR5.

K_n is the transconductance factor of MR5.

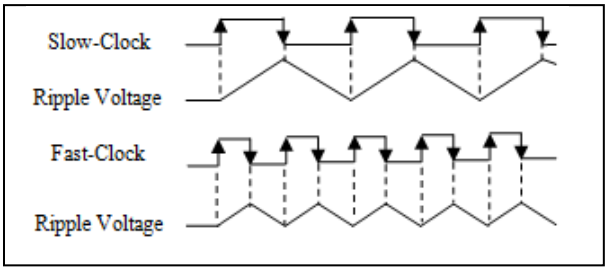


Figure 8: Relation between clock frequency and ripple voltage

The relationships (3) and (4) show that the switching frequency varies linearly with the input signal. The relationship (4) remains valid if the width of MOSFET MR5 is large that it operates in subthreshold region. Consequently its gate-source voltage is always close to V_{thn} regardless of V_{inVCO}. The transfer curve of the CSVCO is presented in Figure 10.

Figure 9a: Schematic of Current Starved VCO

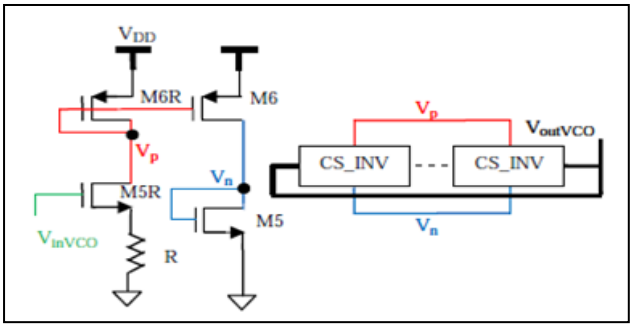


Figure 9b: schematic of Currennt Starved Inverter

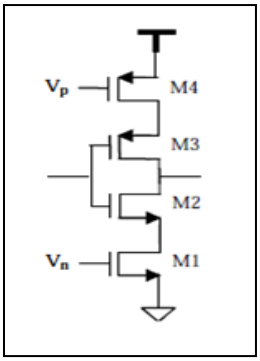
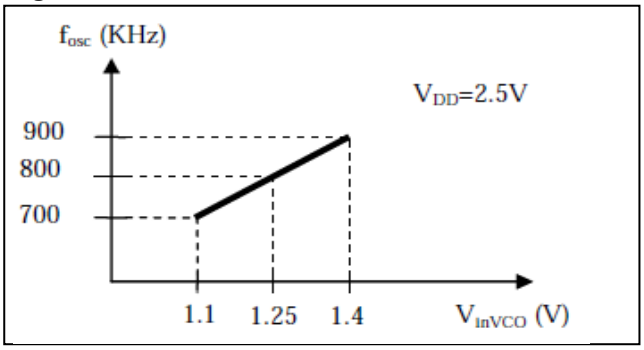


Figure 10: Transfer curve of CSVCO used in this work



4. Simulation results

The proposed regulated charge pump was simulated in 1.2/2.5-V 90-nm CMOS technology using Cadence Virtuoso Spectre Simulator. This circuit can be used to power USB-OTG transceiver. The output voltage of the proposed regulated charge pump can reach more than 4.3-V. As shown in Figure 11, when the load current is 50-mA, the output voltage is 3.8-V and the ripple voltage is 13.22-V. The period of output ripple voltage is 1.26-µs. The power efficiency is higher than 80% regardless of the load current as shown in Figure 12. The dynamic power loss caused by switching large transistor does not change while the load current becomes smaller. As a result, the power efficiency degrades as the load current decreases.

The power efficiency in a steady state was measured using the expression:

$$\xi = \frac{V_{OUT} I_{OUT}}{V_{DD} I_{DD}} \quad (5)$$

When I_{DD} is the current consumption during rise time on the pumping period.

Figure 11: Measurements results of output ripple voltage

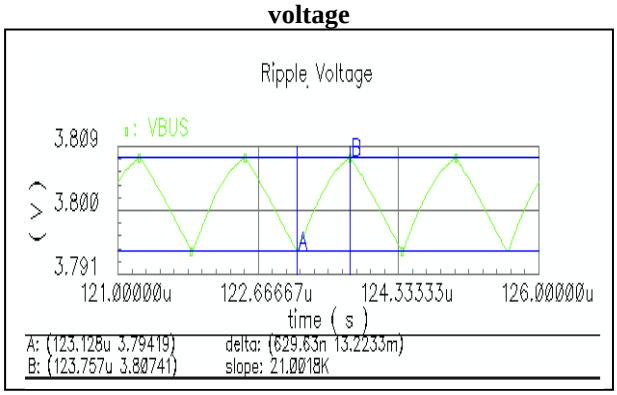


Figure 12: Measurements results of power efficiency

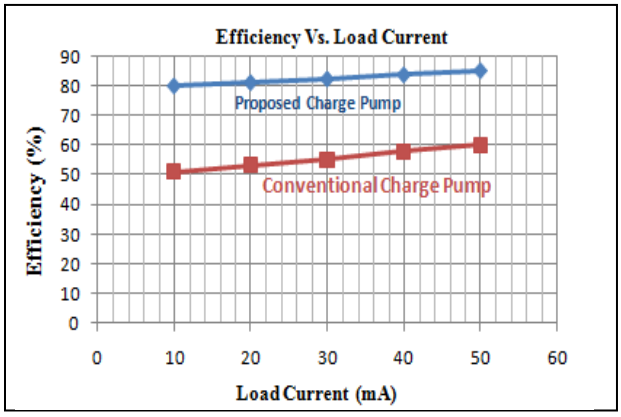


Table I summarizes performance characteristics of the proposed regulated charge pump.

Table I. Performance summary

Low Supply Voltage	1.2-V
High Supply Voltage	2.5-V
Pumping Frequency	700-Khz – 900Khz
Output Voltage	3.8-V ~ 4.3-V
Maximum Load Current	50-mA
Ripple Voltage	13.2-mV (with 2.2-µF load capacitor)
Efficiency	80% ~ 85%
Technology	1.2/2.5-V 90- nm CMOS technology

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